REMARKS

This amendment responds to the office action mailed May 19, 2004. In the office action the Examiner:

- rejected claims 1, 6-9, 17, 22, 23, 28 and 30-32 under 35 U.S.C. 102(b) as anticipated by Dillon et al. (US 5,663,661); and
- objected to claims 2-5, 10-16, 18-21, 24-27 and 29 as being dependent upon a rejected base claim.

After entry of this amendment, the pending claims are: claims 1, 3-14, 16-19, 21-35. The total number of pending claims, 32, remains unchanged.

It is noted that the changes to claims 1, 8 and 17 have been made to advance prosecution, and do not constitute an admission that the Examiner's rejections of those claims were properly based on the prior art of record. The Application reserves the right to resubmit those claims, or similar claims, in one or more continuation applications.

Overview of Changes to Claims

Independent claim 1 has been amended to incorporate the limitations of claim 2. (Claim 2 has been canceled.)

Independent claim 8 has been amended to incorporate the limitations of claim 15. (Claim 15 has been canceled.)

Independent claim 17 has been amended to incorporate the limitations of claim 20, with a correction in the phrasing of the limitation from claim 20. (Claim 20 has been canceled.)

Minor changes have been made to claims 9, 11, 13, 18, 23 and 25 to correct minor errors in antecedent basis and the like

Dependent claim 9 has been amended to clarify that the divide-by-N circuit is an divide-by-N effective-frequency circuit. Support is found in the specification on p. 6, lines 14-19 and lines 24-25. Dependent claim 23 has been amended to clarify that the phase signal is generated as an effective-frequency-divided clock signal. Support is found in the specification on p. 6, lines 14-19 and lines 24-25. As a consequence, no new matter is introduced by these amendments.

New independent claim 33 is the same as previously pending claim 29, except that the names of the signals have been generalized (e.g., "first" and "second") and the terms "master device" and "slave device" have been replaced by "first device" and "second device".

New independent claim 34 is the same as previously pending claim 11, except that the names of the signals have been generalized (e.g., "first" and "second") and the terms "master device" and "slave device" have been replaced by "first device" and "second device".

New independent claim 35 is the similar to previously pending claim 25 (without intervening claim 22), except that the names of the signals have been generalized (e.g., "first" and "second") and the terms "master device" and "slave device" have been replaced by "first device" and "second device".

All pending claims now correspond to claims previously noted by the Examiner as being patentable over the prior art of record.

The six pending independent claims are claims 1, 8, 17, 33, 34 and 35.

Claim 1, as amended, corresponds to previously pending claim 2, which was noted by the Examiner in the office action as being allowable if rewritten in independent form.

Claim 8, as amended, corresponds to previously pending claim 15, which was noted by the Examiner in the office action as being allowable if rewritten in independent form.

Claim 17, as amended, corresponds to previously pending claim 20, which was noted by the Examiner in the office action as being allowable if rewritten in independent form. It is noted that the text from claim 20 has been revised as follows:

> producing a receive clock signal having a frequency determined by said clock signal and <u>a phase determined by</u> said phase-from master signal. (change underlined).

This change is consistent with the specification and improves clarity.

Claim 33 is allowable for the same reasons as previously pending claim 29.

Claim 34 is allowable for the same reasons as previously pending claim 11.

Claim 35 is allowable for the same reasons as previously pending claim 25.

All other pending claims depend from the claims mentioned above, and are allowable at least for the reasons stated above.

Comment Concerning 35 USC 102 (b) Rejection
of Claims 1, 6-9, 17, 22, 23, 28 and 30-32

The previously pending independent claims all required the generation or receipt or use of three distinct timing signals

Independent claim 1 in the present application contains the limitations of three distinct timing signals on three distinct nodes. Specifically,

"... the externally-provided clock signal, the phase-to-master phase signal and the phase-from-master phase signal are **distinct signals** received at **distinct nodes** of the slave device" [emphasis added].

Referring to Fig. 1 of Dillon et al., slaves 115a through 115n, as well as slaves 125a through 125n, each have three nodes, such as d1, t1 and r1 for slave 115a. However, only t1 and r1 are timing-signal nodes. d1 is a data node (col. 4, line 13). The Examiner's argument that rsk1 and/or tsk1 constitute a node for the slaves is erroneous. rsk1 and tsk1 are connections to module 120 (col. 3, lines 55-58). They are not distinct nodes for each slave. Furthermore, the Examiner's argument that a third distinct timing signal is present at rsk1 and/or tsk1 is also erroneous. The timing signals present at rsk1 and tsk1 are clock-to-master and clock-from-master signals from module clock net 166, as well as clock-to-master and clock-from-master signals from motherboard clock net 165. All of these signals are generated by clock generator 130. (Note that there is no separate phase generator in Dillon, as is also required in the limitations of claim 1). The clock-to-master and clock-from-master signals on module clock net 166 and motherboard clock net 165 are, therefore, not distinct.

Dillon et al. does not teach each of the limitations of claim 1. As a consequence, Dillon et al. does not anticipate claim 1 in the present application. Since claims 6, 7, 30 and 31 depend from claim 1, they are also novel with respect to the cited prior art.

Independent claim 8 in the present application contains the limitations of a clock signal generator and a phase signal generator:

"a **clock signal generator** configured to produce a clock signal;

a **phase signal generator** configured to produce a phase signal, wherein said phase signal is distinct from said clock signal ..." [emphasis added].

In addition, there are limitations for separate clock and phase lines connected to the clock signal generator and phase signal generator, respectively, as well as three timing signals. Specifically,

"... a clock line connected to said clock signal generator to carry said clock signal;

a **phase line connected to said phase signal generator** to carry said phase signal, said phase line including a phase-to-master path to carry a **phase-to-master phase signal** and a phase-from-master path to carry a **phase-from-master phase signal** ..." [emphasis added].

Dillon et al. has a clock generator. It does not, however, have a phase signal generator. There are, therefore, no phase lines connected to a phase signal generator in Dillon et al. Furthermore, the clock-to-master and clock-from-master signals, for example on motherboard clock net 165 are generated by the clock generator 130. As a consequence, in Dillon et al. there are two distinct timing signals. Claim 8 has been amended to clarify that there are three distinct timing signals.

Dillon et al. does not teach each of the limitations of claim 8. As a consequence, Dillon et al. does not anticipate claim 8 in the present application. Since claims 9 and 32 depend from claim 8, they are also novel with respect to the cited prior art.

That stated, the Examiner's rejection of claim 9 is also erroneous. Dillon et al. does not disclose the generation of a phase signal from the clock signal. In addition, Dillon et al. does not disclose a frequency divider. Resistors 640 and 680 in Fig. 6 of Dillon et al. constitute a voltage divider. Claim 9 has been amended in the present reply to clarify that the divide by N circuit produces a phase signal with an effective frequency.

Independent claim 17 in the present application contains the limitations of generating a clock signal and a phase signal resulting in three distinct timing signals. Specifically,

"generating a **clock signal** and a **phase signal,** said phase signal **including a phase-to-master signal** and a **phase-from-master signal,** wherein said phase signal is distinct from said clock signal" [emphasis added].

As noted in the previous discussion in the present reply, Dillon et al. neither discloses the generation of both clock and phase signals nor distinct clock and phase signals. In addition, Dillon et al. only has two timing signals, clock-to-master and clock-from-master, for example on motherboard clock net 165 in Fig. 1, generated by clock generator 130. Claim 17 has been amended in the present reply to clarify that the clock signal and phase signal in the present invention are distinct.

Dillon et al. does not teach each of the limitations of claim 17. As a consequence, Dillon et al. does not anticipate claim 17 in the present application. Since claims 22 and 23 depend from claim 17, they are also novel with respect to the cited prior art.

That stated, the Examiner's rejection of claims 22 and 23 is also erroneous. Dillon et al. does not disclose the generation of a phase signal from the clock signal (the limitation of claim 22). In addition, Dillon et al. does not disclose a frequency divider. Resistors 640 and 680 in Fig. 6 of Dillon et al. constitute a voltage divider. Claim 23 has been amended in the present reply to clarify that the divide-by-N circuit produces a phase signal with an effective frequency.

The applicants also note that Examiner's statement that features of the present invention, i.e., transmitting data using the clock signal and the phase-to-master signal and receiving data using the clock signal and the phase-from-master signal, are not claimed is incorrect. Specifically, claim 17 sates:

"at the slave device, transmitting data to a master device **in response to said clock signal and said phase-to-master signal**; and
at the slave device, receiving data from said master device **in response to said clock signal and said phase-from-master signal**" [emphasis added].

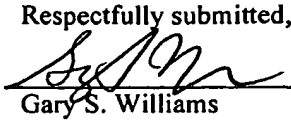
Since Dillon et al. does not anticipate any of the claims in the present invention, withdrawal of this ground for rejection is respectfully requested.

CONCLUSION

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at 650-843-7501, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: January 3, 2005



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